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Synchronous Elastic Systems and Voltage Droop Optimization Using Stochastic Petri Net Model

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ABSTRACT

Electric power systems play a significant role in modern society, serving billions of people. Therefore, there has been growing concern about the reliability and efficiency of the existing power systems; utilities are looking for technology to alleviate their concerns. One of the major concerns associated with voltage demand, is about system strength. System strength refers to the ability to withstand fault events, to maintain and control voltage waveform following these events. This paper aims to fill this gap by introducing synchronous elastic systems, using the SPN model, a connection strategy to improve frequency and voltage stability. In order to reach a more precise control effect, two working cases are considered for demonstrating the proposed control algorithm – droop control using SPN model. Droop control is realized by simulating the droop characteristics of generators and controlling the output voltage and frequency of the voltage source inverter (VSI) according to output power variation. Petri nets are classical tools for modelling and analyzing discrete event systems which are too complex to be described by automata or queuing models. The structural mechanism of the controller is based on the SPN model, which improves the problem of static error in the control of AC variables. The frequency domain characteristics are compared in detail and relevant parameters are designed. Controlling harmonic voltage levels within specified limits at the weakest point on the network ensures that other network locations will have better performance, hence, this study is highly appreciated.

INTRODUCTION

The evolution of technologies enables the integration of complex systems in a single chip (System on-Chip, SoC), and it has brought the popularization of multi-cores (Venkateswaran *et al.*, 2023). As designs have become increasingly complex, Electronic Design Automation (EDA, aka Computed Aided Design, CAD) has rapidly increased in importance. Elastic systems (ES) offer a simple and elegant approach to tolerate variability in computation and communication delays. An ES is a set of computational nodes interconnected by communication channels. The main property of the computational nodes in an ES is that they synchronize their behavior by local hand-shake protocols (Ramos *et al.*, 2023). That is, the behavior of a particular node depends only on its neighbors (Fiiger *et al.*, 2022). This is an example of the optimization opportunities that are enabled by elasticity.

Synchronous Circuits

Figure 1(a) shows a very common abstraction for synchronous circuits. A synchronous circuit is formed by sequential elements (aka state signals), which are synchronized by an external clock, and the combinational logic, which performs the actual computation. The sequential elements load a new stable state each time a clock edge is delivered. The clock signal provides a time reference to the circuit (Leonys *et al.*, 2020), as shown in Fig. 1(b). Between two consecutive edges of the clock, the combinational elements compute the next stable state. Signals need some time to settle to their new state before a new clock edge can arrive. Otherwise, the results can be incorrect. The minimum time distance between two consecutive clock edges is the cycle time of the design, and it determines the maximum clock frequency at which the circuit can run. The slowest timing path determines the cycle time, known as the design's critical path.

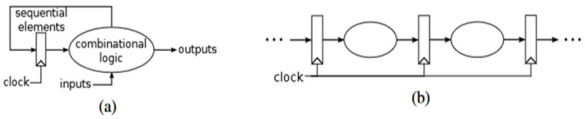

Figure 1(a): A Synchronous Circuit Figure 1(b): A Synchronous pipeline

Retiming and Recycling

The elastic design accepts a set of correct-by-construction transformations. Let us exemplify retiming and recycling

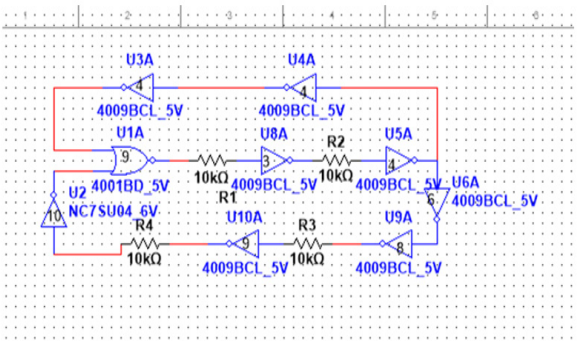

Figure 2A: Simple Elastic Circuit

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transformations. Consider a simple elastic circuit depicted in Figure 2(A). The circuit has nine gates and four registers, (UA1, U8A, U5A, U4A, U3A, U6, U9A, U10A, & U2) while the registers are labeled as R1,R2,R3,R4.
This means that all of them store some valid data. This dot helps to distinguish valid data (tokens) from non-valid (bubbles). Each gate is labeled with the corresponding combinational delay. The control module of the circuit is not shown in the figure, since we are interested only in its data-path. The longest combinational path of the circuit (critical path) is formed by the nodes (U5A, U4A, U3A & U1A): its total delay is equal to 4 + 4 + 4 + 9 = 21 units of time. Thus, 21 can be used to estimate the performance of the circuit. Retiming, a classical optimization technique of synchronous design, can also be applied to elastic design. Retiming moves registers across combinational nodes of the circuit, changing its critical paths while preserving sequential behavior. In the example, one can move register R1 backward across node A. This leads to the configuration with two registers R1A and R1B, as it shows Figure 2(B).

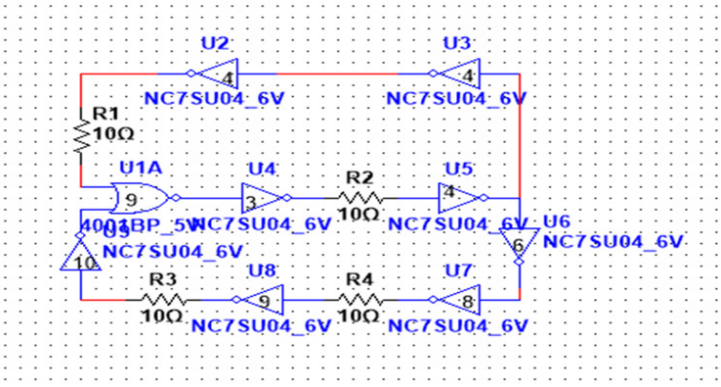

Figure 2B: Retiming and Recycling Circuit Transformation

The critical path of this configuration would be formed by the nodes (U5, U6, U&) thus providing performance measure of 18 units of time. Figure 2(b) shows an optimized version of the circuit after applying both retiming and recycling transformations. The main limitation of the retiming is that it preserves the number of registers at each directed cycle of the retiming graph [84]. C-slow transformation overcome this limitation making c copies of each register. The following transformations were performed on the original circuit: retiming register R1 backward across combinational block and placed to the inputs of this node, resulting in registers R1 and R2; putting a bubble, denoted as B, to further break long combinational paths. It can be verified that now the critical path has delay of 12 units of time. There are two paths with such delay: $(U1 \rightarrow U4)$ and $(U5 \rightarrow U3 \rightarrow U2)$ (Seongmun *et al.*, 2023). One of the main contributions of this work is an algorithm to apply retiming and recycling to achieve the best possible performance of elastic circuit.

Statement of the Problem

The synchronous design principle assumes that the signal propagation through the combinational logic is complete before the next active clock edge. Temperature and voltage variations lead to dynamically changing interconnect and transistor delays, and are classically alleviated by decreasing the clock frequency such that a single clock period always provides sufficient time, even in face of worst-case temperature and voltage conditions. These effects, together with worst case assumptions on aging and process variation, lead to a large frequency guard band that results in underutilization of the circuit under normal conditions.
However, as nano-technology continues to scale down, the uncertainty of the delays increases and timing is becoming wire dominated. If a communication is required between two nodes that are situated far apart on the chip, it can take a long time. To meet the timing requirements for this communication, the cycle period may need to be increased, thereby, degrading the performance of the circuit.
Naive handling of supply voltage droops in synchronous circuits results in conservative bounds on clock speeds, resulting in poor performance even if droops are rare. In general, the response time greatly limits the frequency of a typically sin-shaped droop that can be tolerated in the worst case: assume that a circuit is of the form that it has to sense a low VDD voltage and has response time of k- clock cycles with period T. Given the fact that the sin reaches its minimum after 1/4th of its period, and requiring the circuit to react roughly within this time, the worst-case droops that can be tolerated must have a frequency of less than $1/(4 \cdot k \cdot T)$; rendering response time the major limiting factor of such designs.

Stretchable Clock

The main motivation behind machines with stretchable clocks has been to avoid the metastability problems. Stretchable clock can stretch a clock phase for an unbounded period of time. In the meanwhile, inputs and outputs will become valid. Therefore, they are suitable for interaction with the global asynchronous characteristics. The stretchable clock consists of a ring oscillator as shown in figure 3. For safety and reliability of the clock a Muller C-element is been used. If STRETCH is not asserted to low, the output and inputs of the C-element

will follow the signal transitions. If STRETCH is asserted to high, the input is set to low, the output of the C-element could be either low or high. The output will eventually be maintained at a low level. The next rising edge is postponed the STRETCH+. An OR gate is used for multiple requests for stretching the clock (Rong *et al.*, 2020).

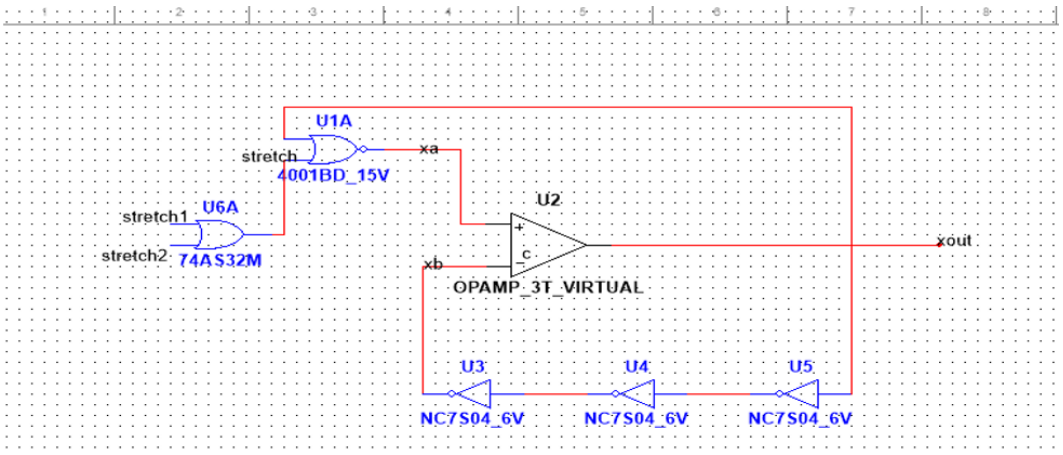

Figure 3. Stretchable clock generation.

Petri Nets

Petri nets are a well-known mathematical model use to describe distributed systems. A Petri net (see Grobelna & Karatkevich, 2021)is a directed bipartite graph formed by transitions, which model events and are drawn as a bar, and places, which model conditions and are drawn as a circle (see figure 4A).

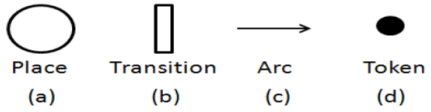

Figure 4A. Petri net basic elements

The arcs of the net connect transitions to places and places to transitions. Places can contain a natural number of tokens. A marking assigns a number of tokens to each place. More formally, a Petri net is a 4-tuple

$$P = (P, T.F, M_0)$$

where:

Figure 4B: Petri net before and after firing transition t.

P is a finite set of places, $p_1, p_2, ..., p_m$

T is a finite set of transitions, $t_1, t_2, ..., t_n$

$F \subseteq (PxT) \cup (TxP)$ is a set of arcs,

$M_0 : P \to N$ is the initial marking, which assigns a number ot tokens to each place. The preset of a transition t is the set formed by its input places,

$$^*t = \{p \in P \mid (pxt) \in F\}$$

Post set is the set formed by its output places,

$$t^* = \{p \in P \mid (t, p) \in F\}.$$

A transition t is said to be enabled if each of its input places is marked with at least one token. When an enabled transition fires, one token is removed from every input and one token is added to every output. Figure 4B shows the marking of a Petri net before and after firing transition t.

Voltage Drop / Voltage Droop

The scenario here is that a circuit that has a few different resistances, like the one shown below (figure 5). V is the voltage source, and R1, R2, and R3 are resistors. There is a current, I, flowing through the circuit that will meet each of these resistances.

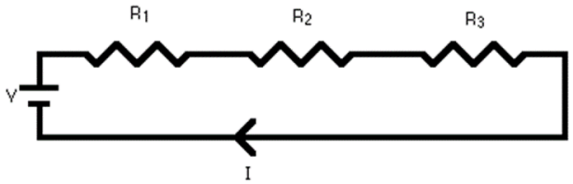

Figure 5: Voltage Drops and Voltage Droop Scenario

The main key is to understand what voltage is. Voltage is just a way to describe how much energy is supplied from a source. You can kind of think of it as an electric potential energy. This energy is traveling in the form of current and meets disturbances along its path, called resistances. The larger the resistance, the more energy it takes to get through that resistance, and as a result, it loses that energy which is dissipated as heat. So, after every resistance the current goes through, it loses energy through heat dissipation, and thus experiences a drop in

energy/voltage. The larger the resistance, the larger the amount of energy it needs to use in order to get through. A voltage drop just describes how energy is reduced as it goes through a resistance (Fredrick *et al.*, 2011).

Let's start with the most basic high-school physical science class equation for charge in a capacitor:

$$Q = CxV \quad (1)$$

$$Q = charge(coulombs)$$
$$C = capacitor(farads)$$
$$V = voltage(volts)$$

Introducing the knowledge of calculus:

$$I = \frac{\partial Q}{\partial t} = Cx\frac{\partial v}{\partial t} \quad (2)$$

Where:

$$I = current..(amperes)$$

Now we rearrange the equation to solve for the "Ccs" which is the required charge storage:

$$C_{cs} = \frac{I}{\frac{\partial v}{\partial t}}(farads) \quad (3)$$

Where :

$$I = current(in.amperes)$$
$$\partial v = allowabe.voltage.drop$$
$$\partial t = pulse.width$$

Let's restate the equation in units that make more sense for microwave modules (micro-Farad and microseconds) and replace the derivative format with deltas which make us feel more comfortable:

$$C_{cs} = \frac{Ix\Delta t}{\Delta v}(micro - farads) \quad (4)$$

$$I = current(amperes)$$
$$\partial v = allowable.voltage.drop(volts)$$
$$\partial t = pulse.width(seconds)$$

Figure 6A shows an equivalent circuit schematic for a current transformer with load RL The parasitic components, Rs, Lkp, and Lks, all act to lower the output voltage across RL, hence the output voltage, Vout, will not equal the induced secondary voltage Vsi. Rs and Lks act in series with RL and are reflected to the primary side along with Rs. Their presence presents added impedance to the primary current hence an increase in primary voltage in proportion to the impedance. Consequently, RL still has the same voltage drop and current flow as it did without Lks and Rs even though Vs does not equal Vout. The phase shift associated with Lks will cause some slight deviation from the ideal current ratio (which equals the turns ratio).

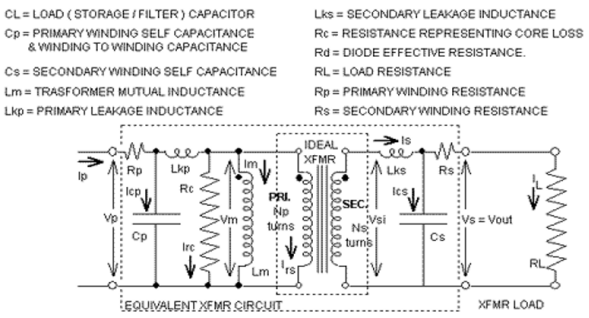

Figure 6A: Voltage Droop Topology

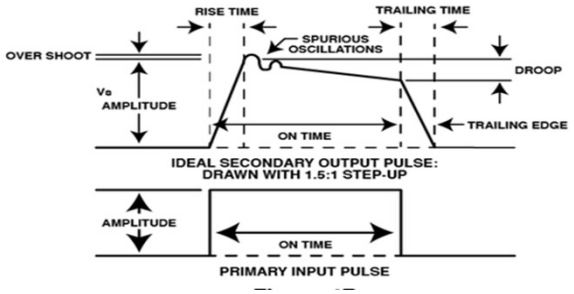

Figure 6B: Graphical illustration of Droop Voltage

For R_p=0 the source voltage (depicted in figure 8A) divides proportionally across Lkp and Lm hence the voltage across Lm can be defined as Vm where V_m=(vxL_m)/(L_m+L_{kp}). The induced secondary voltage becomes equal to (Ns x Vm) / Np. For R_p > zero a voltage drop occurs across R_p . The value of this drop increases in value as the primary current increases with time, hence Vm decrease over time and consequently the secondary voltage declines over time. Thus, R_p and magnetizing current contribute to secondary voltage droop. Lkp does not contribute to the droop in the no-load case but does contribute to a lower secondary starting voltage for both the no load and under load cases. Droop is graphically illustrated in Figure 6B. The conservation of energy requires that the output power equals the input power, hence (Vp x Ip) must equal (Vs x Is). Since Vs = (Vp x Ns) / Np, it can be shown that Is = (Ip x Np) / (Ns x Is) = (Vs / RL), hence Ip = (Ns x Vs) / (RL x Np). Rp and Lp are primary side resistance and leakage reactance of transformer. Rs and Ls are for the secondary of transformer. Rc and Lm are the core loss component and magnetizing reactance component respectively. Error is mainly introduced in the measurement of voltage and phase angle due to these parameters of transformer (Mingshen et al., 2022). The voltage transformers have a specified rated transformation ratio. If k_n is the rated transformation ratio then voltage error in percentage is given as,

$$Voltage.Error = \frac{(k_n * V_s - V_p)}{V_p} x100 \quad (5)$$

where.V_p & V_S are the actual primary and secondary voltage parameters of transformer. We Know the two fundamental laws of the inductive transformer. For an ideal transformer (Leonys et al., 2020),

$$\frac{V_p}{N_p} = \frac{V_s}{N_s} and.. \frac{I_p}{N_p} = \frac{I_s}{N_s}$$

Subscripts 'p' and 's' are used for primary and secondary sides of the transformer. N is the number of turns of the respective side of the transformer.

The voltage droop is the sum of all the individual voltage drops in the distribution network between the transmission network represented by the voltage source and the observed network point. The total voltage drop of the network is the sum of the voltage drops between the transmission network and the low voltage end at the remote end of the network. The voltage drop represents a complex interaction between distributed loads that affect the impedance configuration of the network (Mingshen et al., 2022).

LITERATURE REVIEW

The energy sector is undergoing major transformation, shifting from conventional synchronous generators (SGs) to renewable energy sources (RESs). The rapid growth of RES connections to power networks has created great stability challenges. The majority of RESs are connected to the grid through inverters, and consequently, they are not mechanically coupled with the grid, resulting in greater sensitivity to disturbances where the RESs are connected (Mariachet *et al.*, 2019). One of the major concerns associated with the high penetration of RESs is about system strength. System strength refers to the ability to withstand fault events, and to maintain and control voltage waveform following these events (Fugger *et al.*, 2020). The strength of a system is proportional to the amount of fault level available at the point of connection, whereby increasing the fault level at a location result in increased strength and stability. Considering stability concerns associated with weak grids, planning connections of assets, such as battery energy storage systems (BESSs), is very important. This paper aims to fill this gap by introducing synchronous elastic systems, a connection strategy to improve both frequency and voltage stability in weak grids.

In order to reach a more precise control effect, a PCI (proportional complex integral, PCI) controller is proposed (Lu & Liu, 2022). The structural mechanism of the controller is based on the PI controller, which improves the problem of static error in the control of AC variables. The frequency domain characteristics of the above two are compared in detail, and the relevant parameters are designed (Fu *et al.*, 2020). With the increase in global population, the demand for electricity is increasing. The rise in the electricity demand increases the possibility of a power mismatch and increases the system marginal price of the commodity, which could lead to economic losses (Fernando *et al.*, 2022). Electric power systems play a significant role in modern society, serving billions of people. Therefore, there has been growing concern about the reliability and efficiency of the existing power systems; utilities are looking for technology to alleviate their concerns (Fugger *et al.*, 2022). Traditionally, fossil fuel power generators are used to manage the electricity supply and demand, but this approach is expensive and causes high carbon emissions.

An energy storage system (ESS) can increase the system flexibility to alleviate the growing demand. Not only can the ESS respond quickly to changes in the systems but it also enables the storage and supply of electrical energy at required times (Giambattista *et al.*, 2020). These features make ESSs promising candidates for a wide range of power system applications (e.g., energy arbitrage, peak shaving, frequency regulation, and renewable integration) (Hooman *et al.*, 2023). In the application of variable renewable energy (VRE) integration, ESS can play significant role for reducing the VRE's variability caused by its uncertainty and intermittent nature. Moreover, ESS provides the opportunity for customers to manage their demand, resulting in additional benefits to customers. Consequently, ESS can be utilized for economic viability and improvement of system reliability and load profile (Wang *et al.*, 2023). This has not help this study because of its uncertainty and intermittent nature.

As designs have become more and more complex, Electronic Design Automation (EDA, aka Computed Aided Design, CAD) has rapidly increased in importance (Mehrasa *et al.*, 2023). During the early years of the semiconductor industry, integrated circuits were designed by hand and the layout was also built manually. Incrementally, more and more stages of design were performed in an automatic or semiautomatic way. Place and route tools appeared, hardware description languages, verification tools, simulation tools, logic synthesis, etcetera. Today, EDA is present in all stages needed to build an integrated circuit: design (from high level synthesis to physical synthesis), simulation, analysis, verification and manufacturing. However, since technologies continue to shrink, the known problems become more challenging and new problems emerge. While synchronous circuits have been the dominant paradigm for circuit design through all these years, the asynchronous alternative has always been there claiming to provide a possible solution for the dark clouds that hover over the synchronous world. Synchronous elastic systems have emerged in the last years as a middle ground solution between synchronous and asynchronous circuits (Mehmood *et al.*, 2023). They can be designed and implemented using regular synchronous flows and tools, but they provide some of the advantages of asynchronous designs since they can tolerate variations in the latencies of the computations and the communications.

This tolerance can be used to separate performance critical parts from non-critical and optimize the former ones in isolation, while non-critical parts are removed from critical paths by adding latency to their computations. This is an example of the optimization opportunities that are enabled by elasticity. This study works in line with these authors and proposes a framework to leverage synchronous elastic systems in order to perform design

space exploration of microarchitectures automatically (Fu-Bao *et al.*, 2019).

In a pipelined system each instruction needs several pipeline stages to be executed, but several instructions can be executed simultaneously. Pipelining may increase the performance of the system. The unacceptability of long wires further motivates the development of pipelined architectures. However, building a good pipeline from a non-pipelined design is a challenging task (Mariachet *et al.*, 2019), while the pipelining of the elastic design can be automated. All these potential benefits of the elastic design motivated this study to investigate in depth using stochastic Petri nets model. There are a lot of publications in the area of elastic design itself. Power supply plays a central role when designing the guard band: Sensitivity of gate propagation delay increases (Grobelna *et al.*, 2021). The trend to decrease VCC suggests that the situation will gain in importance for future chip generations. In (Fugger *et al.*, 2022) it was shown that a major part of the guard-band is required to account for power supply noise, with more than 6% loss in attainable clock frequency for a 130 nm processor. In (Roberto *et al.*, 2019), a 12% voltage droop at 100MHz was injected into a 45 nm microprocessor, already requiring a 16% reduction of clock frequency to account for increased critical path delay. Several techniques for handling slowly changing environmental conditions have been proposed, ranging from slow temperature-voltage and aging compensation (Frederic *et al.*,2011) to process variation compensation (Fernando *et al.*, 2022). However, compensation techniques typically involve significant sensing and response times that prevent their application for fast environmental changes with dynamics in the order of a single clock period.

METHODOLOGY

Droop Control Method

Droop control is a method used for the control of distributed power that mimics operation of conventional SG behavior. It is used in load sharing and main regulation of the frequency, while the emulated behavior of the virtual inertia is not considered when you model the droop control. The voltage capacitor at the DC oscillates without contribution from storage energy, which causes problems in the stability of the power system. Two RES are connected through energy converters, as shown in figure 9. The droop control method is often applied (Majid *et al.*;2023). The equivalent circuit of two converters connected to common AC microgrid bus is presented by Figure. 7

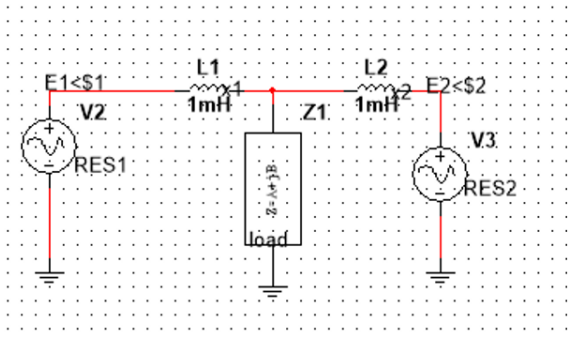

Figure 7: Equivalent circuit of parallel connected VSIs.

Presented scheme is similar to the equivalent circuit of synchronous generator (SG), hence the active and reactive power of k-th converter connected to AC microgrid can be described as:

$$P_k = \frac{E_k V}{X_k} \sin \$_k \qquad (6)$$

$$Q_k = \frac{E_k V \cos \$_k - V}{X_k} \qquad (7)$$

where P – active power, E – converter voltage amplitude, V – voltage amplitude in point of common coupling, X – coupling impedance, $– angle of converter voltage (see Fig.7). Based on above equations it can be assumed, that:

> active power P mainly depends on $, which is changing by ω,

> reactive power Q depends on voltage amplitude E. Hence, the P – ω and Q – E droop characteristics can be drawn (Figure 8).

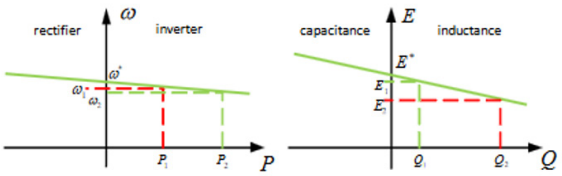

Figure 8: P – ω and Q – E droop characteristics

RESULT AND DISCUSSION

Balanced loads are connected and then a step change of the loads is provided by connecting unbalanced loads after 0.2 seconds (see Fig. 8). The amplitude of the reference phase voltage is set at 310 V with a frequency of 50 Hz. The results show that the load voltages are symmetrical under load variations and very well track the reference voltages with low harmonic distortion. The control approach provides a fast dynamic response which is obvious at the moment of connecting the unbalanced load. The neutral current is zero in the case of a balanced load and starts to flow in the neutral line in the condition of unbalanced load connection. The DC-link capacitor voltage has low ripple level which begins increase with the unbalanced load connection with a percentage ripple not exceeding 2%. Furthermore, the control performance shows good static and dynamic responses with load variations.

Petri Nets Modeling Method

The PN properties allow a detailed analysis of the modeled system. For this, two types of properties have been considered in a Petri net model: behavioral and structural properties. Behavioral properties are those which depend on the initial marking. Structural properties, on the other

hand, are those that are marking-independent (Othman *et al.*, 2021), describes some behavioral properties, since such properties are very important when analyzing a given system.

$$\sigma = t_1, t_2, \ldots, t_n M_i M_0 M_0 [\sigma > M_i M_0 M_0 M_0 M_0 M_0 M_0 L(M_0)$$

Dependability

Dependability of a computer system must be understood as the ability to deliver services with respect to some agreed specifications of desired service that can be fully trusted (Fang *et al.*, 2023). Indeed, dependability is related to disciplines such as fault tolerance and reliability. Reliability is the probability that the system will deliver a set of services for a given period of time, whereas a system is fault tolerant when it does not fail even when there are faulty components. Availability is also another important concept, which quantifies the mixed effect of both failure and repair process in a system. In general, availability and reliability are related concepts, but they differ in the sense that the former may consider maintenance of failed components (Mehmood *et al.*, 2023) (e.g., a failed component is restored to a specified condition If one is interested in calculating the availability (A) of given device or system, he/she might need either the uptime and downtime or the time to failure (TTF) and time to repair (TTR). Considering that the uptime and downtime are not available, the latter option is the mean. If the evaluator needs only the mean value, the metrics commonly adopted are Mean Time to Failure (MTTF) and Mean Time to Repair (MTTR) (other central values might also be adopted). However, if one is also interested in the availability variation, the standard deviation of time to failure (sd(TTF)), and the respective standard deviation of time to repair (sd(TTR)) allow one the estimate the availability variation. The availability (A) is obtained by steady-state analysis or simulation, and the following equation expresses the relation concerning MTTF and MTTR:

$$A = \frac{MTTF}{MTTF + MTTR} \qquad (8)$$

Through transient analysis or simulation, the reliability (R) is obtained, and, then, the MTTF can be calculated as well as the standard deviation of the Time To Failure (TTF):

$$MTTF = \int_0^\infty t f(t)\,dt = \int_0^\infty -\frac{dR(t)}{dt} t\,dt = \int_0^\infty R(t_0)\,dt \qquad (9)$$

$$sd(TTF) = \sqrt{-\int_0^\infty t^2 f(t)dt - (MTTF)^2} \qquad (10)$$

Considering a given period t, R(t) is the probability that the time to failure is greater than or equal to t. Regarding exponential failure distributions, reliability is computed as follows:

$$R(t) = \exp\left\{-\int_0^t \lambda(t')dt'\right\} \quad \textbf{(11)}$$

where λ(t') is the instantaneous failure rate.

One should bear in mind that, for computing reliability of a given system service, the repairing activity of the respective service must not be represented. Besides, taking into account

(unavailability), the following equation is derived:

$$MTTR = MTTF x \frac{\mu A}{A} \qquad (12)$$

$$sd(TTR) = sd(TTF) x \frac{\mu A}{A} \quad (13)$$

Next, MTTF/(sd(TTF) and..MTTR/(sd(TTR) are computed for choosing the expolinomial distribution that best fits the TTF and TTR distributions (Fernando *et al.*, 2023). Figure 12 depicts the generic simple component model using SPN, which provides a high-level representation of a subsystem. One should notice the trapezoidal shape of transitions (high-level transition named s-transition). This shape means that the time distributions of such transitions are not exponentially distributed, instead they should be refined by subnets. The delay assigned to s-transition f is the TTF and the delay of s-transition r is the TTR. If the TTF and TTR are exponentially distributed, the shape of the transitions should be the regular one (white rectangles) and TTF and TTR should be summarized by the respective MTTF and MTTR.

Stochastic Petri Net Model

This section presents a proposed SPN building block for obtaining dependability metrics.

Simple Component

The simple component has two states: functioning or failed. To compute its availability, MTTF and MTTR should be represented. Figure 10 shows the SPN model of the "simple component", which has two parameters (not depicted in the figure), namely X_{MTTF} and $X_{MTTR,}$ representing the delays associated to the transitions X_ Failure and X_{Repair}, respectively.

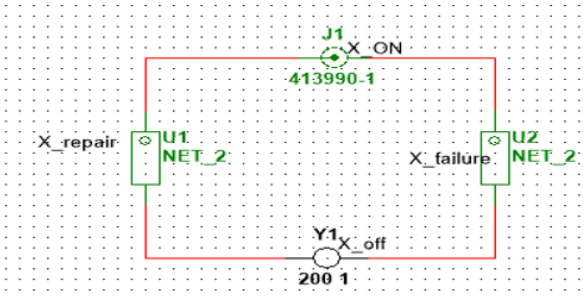

Figure 9: Simple component model

Places X_{ON} and X_{OFF} are the model component's activity and inactivity states, respectively. The simple component also includes an arc from X_{OFF} to X_{Repair} with multiplicity depending on place marking. The multiplicity is defined through the expression IF(#X_Rel_Flag = 1):2 ELSE 1, where place X_Rel_Flag models the evaluation of

reliability/availability. Hence, if condition #X_Rel_ Flag = 1 is true, then the evaluation refers to reliability. Otherwise, the evaluation concerns availability. Besides, although simple component model has been presented using the exponential distribution, other expolinomial distributions that best fits the TTF and TTR may be adopted following the techniques presented in (Fang *et al.*, 2023). Cold standby. A cold standby redundant system is composed by a non-active spare module that waits to be activated when the main active module fails. Figure 11 depicts the SPN model of this system, which includes four places, namely X_{ON}, X_{OFF}, X_Spare1_ON, X_Spare1_OFF that represent the operational and failure states of both the main and spare modules, respectively. The spare module (Spare1) is initially deactivated; hence no tokens are initially stored in places X_Spare1_ON and X_Spare1 _OFF. When the main module fails, the transition X_Activate_Spare1 is fired to activate the spare module. Once considering reliability evaluation (number of tokens (#) in the place X_Rel_Flag = 1), the X_Repair, X_Activate_Spare1 and X_Repair_Spare1 transitions receive a huge number (many times larger than the associated MTTF or MT-Activate) to represent the absence of repair. The MT-Activate corresponds to the mean time to activate the spare module. Besides, when considering reliability, the weight of the edge that connects the place X_Wait_Spare1 and the X_Activate_Spare1 transition is two; otherwise, it is one. Both availability and reliability may be computed by the probability P{#X_ ON = 1 OR #X_Spare1 _ON = 1}.

System Algorithm

1. X_{ON}&X_{OFF} are the model components' activity and inactivity states respectively.
2. Input the main and spare modules.
3. Deactivate the spare module and no tokens stored in places (X_spare1_ON & X_spare1_OFF) can function any more.
4. Test the functionality of the main module and if it fails, is fired to activate the spare module.
5. The X_Repair, X_activate_spare & X_Repair_spare transmissions receive a huge number, greater than the associated MTTF.
6. Power goes through voltage panels, uninterruptible power supply (UPS) and power distribution unit (PDU) .
7. Determine whether the difference between the node voltage and the reference voltage of the node in the system exceeds the set dead zone voltage, and if so, adjust it.
8. Both availability and reliability may be computed by the probability P(#x_ON=1,or#X_spare1_ON=1) X_MTTF & MTTR representing the delays associated to the transitions X_failure&X_repair respectively.
9. According to the set objective function, the tap value that satisfies the normal operation of the system and minimizes the loss is obtained. Simple power system simulation. Taking the simple power system shown in Figure 11 as an example, the load uses a dynamic load model as shown below:

$$\begin{cases} \dot{x}_p = \dfrac{-1}{60} x_p + v - v^2 \\ \dot{x}_q = \dfrac{-1}{60} x_q + 0.2(v - v^2) \end{cases} \quad (14)$$

10. It can be seen from the above figure that the voltage has exceeded the limit, so the voltage in the system is adjusted and controlled according to the proposed method (see figure 10).

Flowchart Algorithm

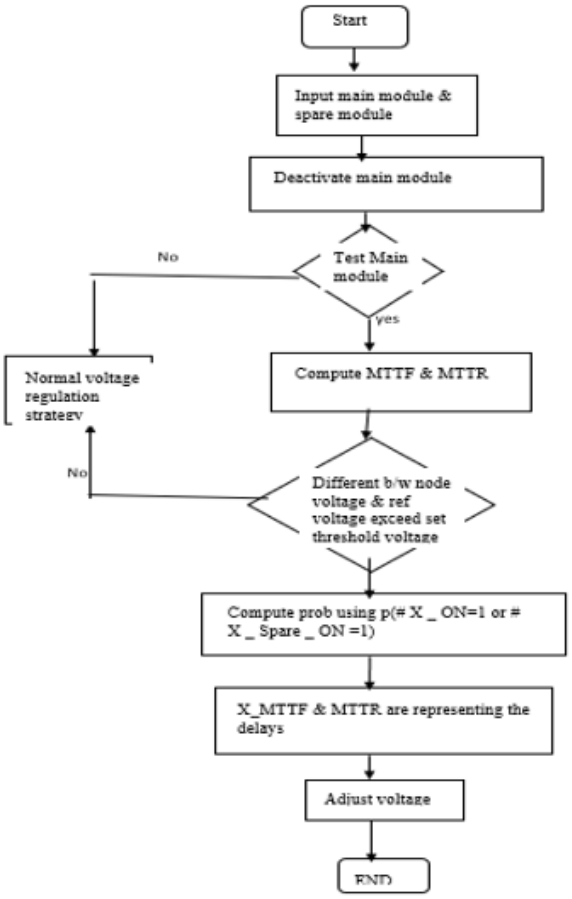

Figure 10: SPN Model Flowchart

RESULT AND DISCUSSION

The simple component has two states: functioning or failed. To compute its availability, MTTF and MTTR is represented. Figure 11 depicts the SPN model of this system, which includes four places, namely X_ON, X_ OFF, X_Spare1_ON, X_Spare1_OFF that represent the operational and failure states of both the main and spare modules, respectively. The spare module (Spare1) is initially deactivated; hence no tokens are initially stored in places X_Spare1_ON and X_Spare1 _OFF. When the main module fails, the transition X_Activate_Spare1 is fired to activate the spare module. . Both availability and reliability may be computed by the probability P{#X_ ON = 1 OR #X_Spare1 _ON = 1}. Determine whether the difference between the node voltage and the reference voltage of the node in the system exceeds the set dead

zone voltage, and if so, adjust it. In order to reach a more precise control effect, the structural mechanism of the controller is based on the PI controller, which improves the problem of static error in the control of AC variables. The strength of a system is proportional to the amount of fault level available at the point of connection, whereby increasing the fault level at a location result in increased strength and stability. Considering stability concerns associated with weak grids, planning connections of assets, such as battery energy storage systems (BESSs), is very important.

CONCLUSION

Elastic systems (ES) offer a simple and elegant approach to tolerate variability in computation and communication delays. The main property of the computational nodes in an ES is that they synchronize their behavior by local hand-shake protocols. That is, the behavior of a particular node depends only on its neighbors. If some input data is not available, the node waits for it as long as necessary to perform a computation.

This paper aims to fill this gap by introducing synchronous elastic systems, a connection strategy to improve both frequency and voltage stability. The first contribution of this work combines retiming (a well-known sequential optimization technique) with recycling (insertion of bubbles) to optimize the performance of ESs. For this, the performance of ESs is modeled with a set of linear inequalities. The main limitation of the retiming is that it preserves the number of registers at each directed cycle of the retiming graph (Jang *et al.*, 2023). C-slow transformation overcome this limitation making c copies of each register. The experimental results showed that the simultaneous application of both techniques helps to achieve better performance. The cycle time of the circuit could be hardly reduced beyond one retiming achieves and never beyond the cycle time that clock skew optimization provides.

The PN properties allow a detailed analysis of the modeled system. For this, two types of properties have been considered in a Petri net model: behavioral and structural properties. Behavioral properties are those which depend on the initial marking. Structural properties, on the other hand, are those that are marking-independent. This study presents a mathematical model for obtaining dependability metrics, hereby referred to as "Simple Component". The simple component has two states: "functioning or failed." In order to reach a more precise control effect, the structural mechanism of the controller is based on the SPN model, which improves the problem of static error in the control of AC variables. Droop control is realized by simulating the droop characteristic of generators in a traditional grid and controlling the output voltage and frequency of the voltage source inverter (VSI) according to variation of the output power. The control strategy is based on inverter parallel-connection technology. The following two working cases are considered for demonstrating the proposed control algorithm. When the network point voltage (PV) causes disconnection, the voltage of each node will change accordingly. If voltage control is not performed, the voltage changes as shown in Figure 9. It can be seen from the above figure that the voltage has exceeded the limit, so the voltage in the system is adjusted and controlled according to the proposed method. The advantage of the synchronous approach is that the design process is significantly simplified.

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